

FIG. 1

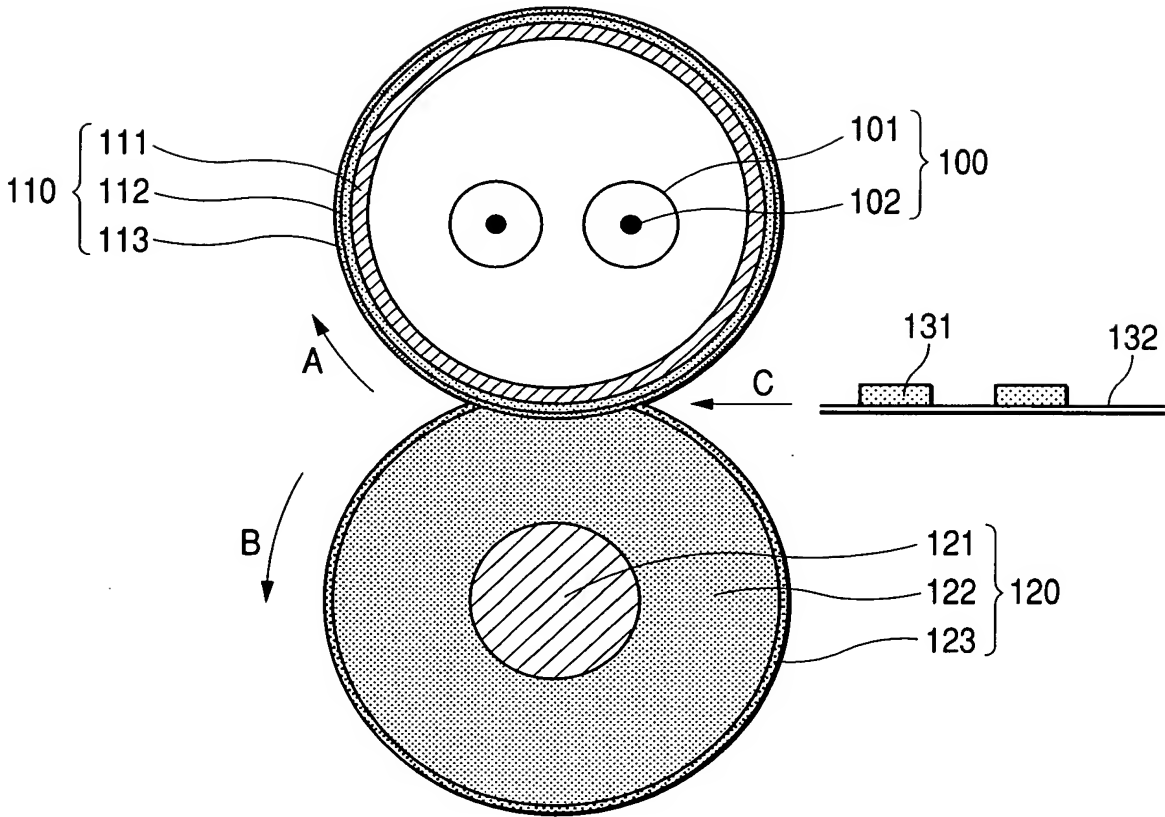


FIG. 2

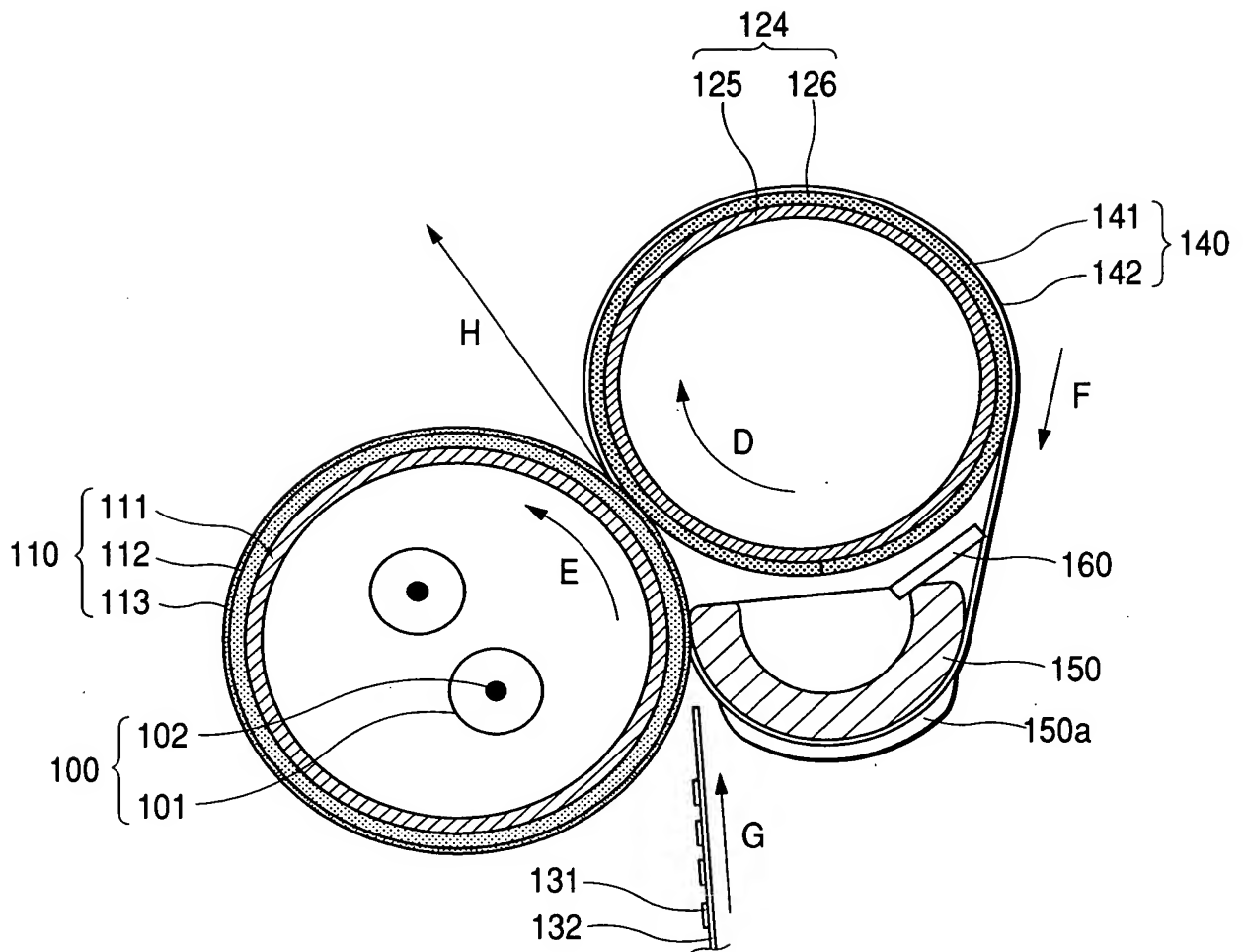


FIG. 3A

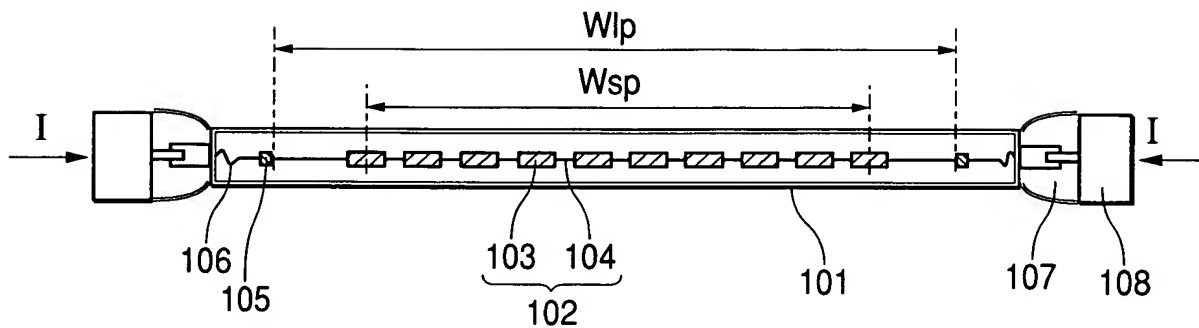
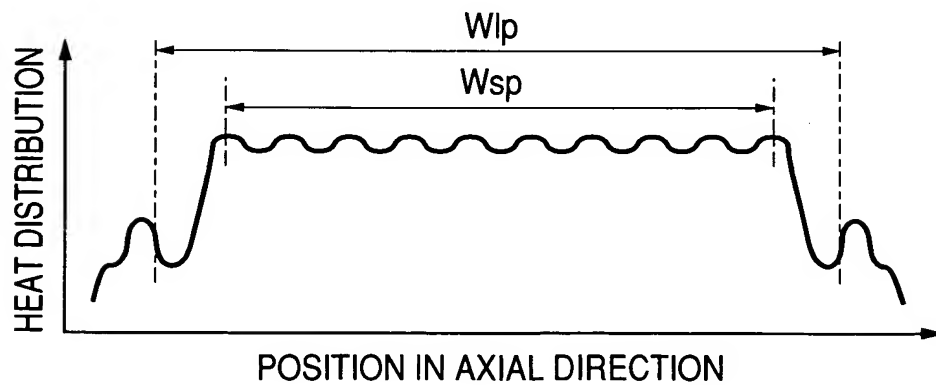
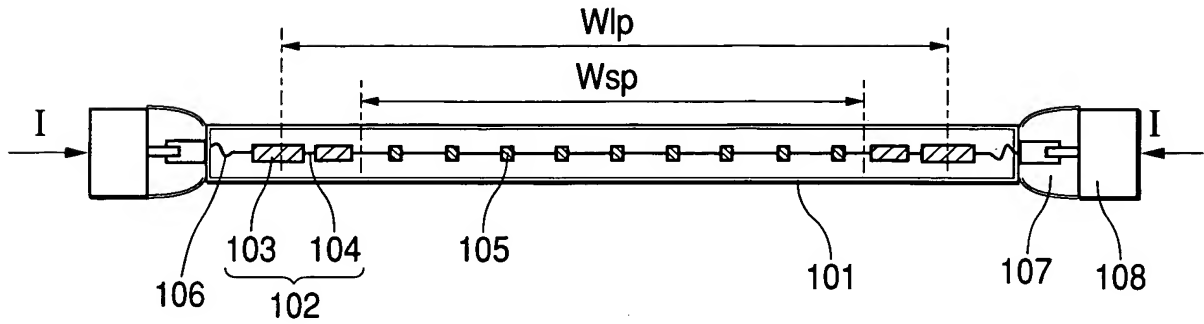


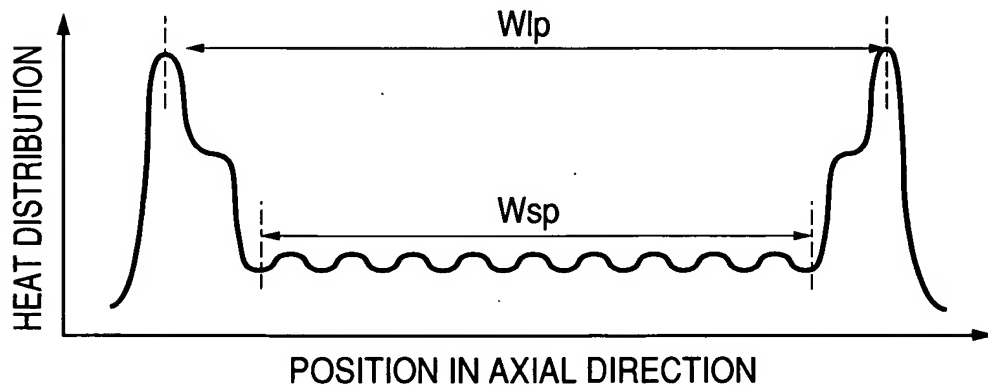
FIG. 3B



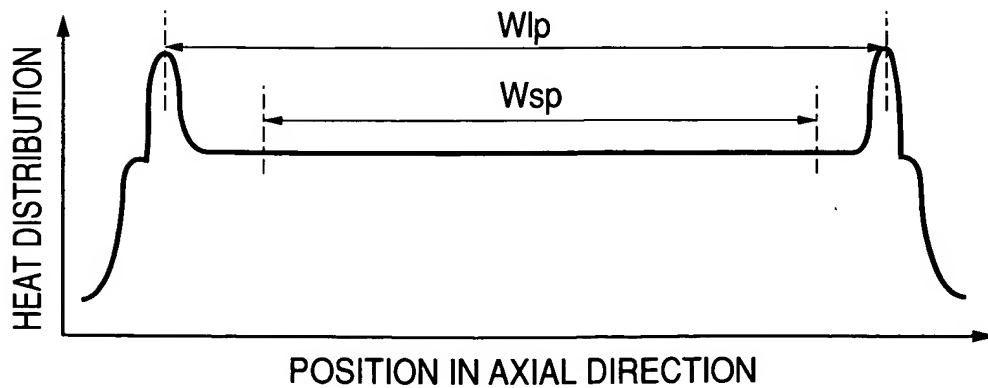
**FIG. 4A**



**FIG. 4B**



**FIG. 5**



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FIG. 6

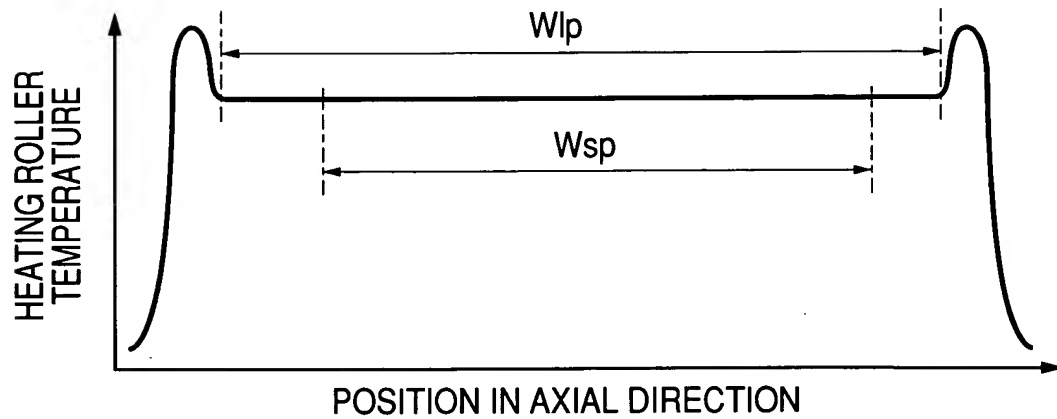


FIG. 7A

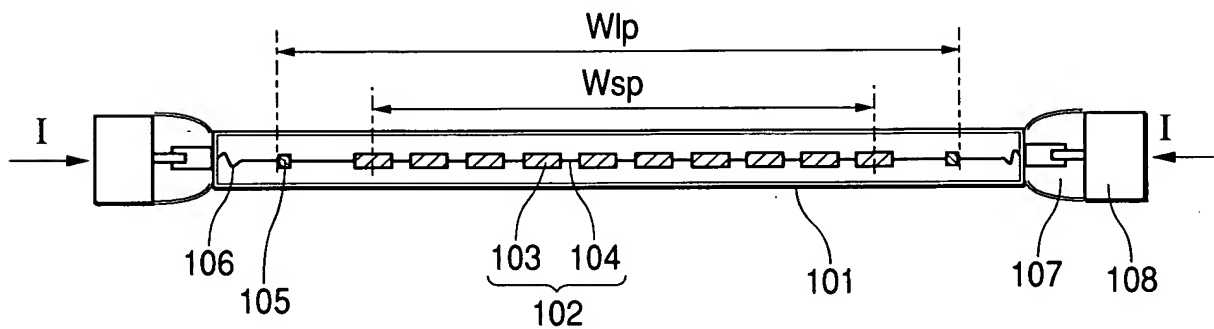
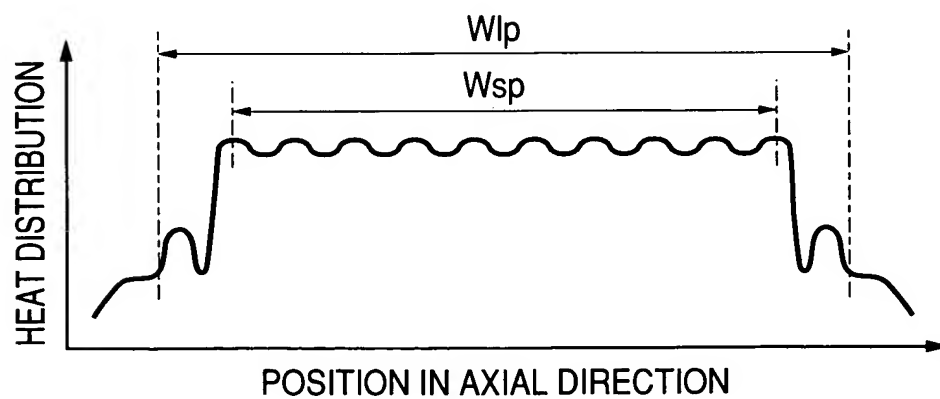
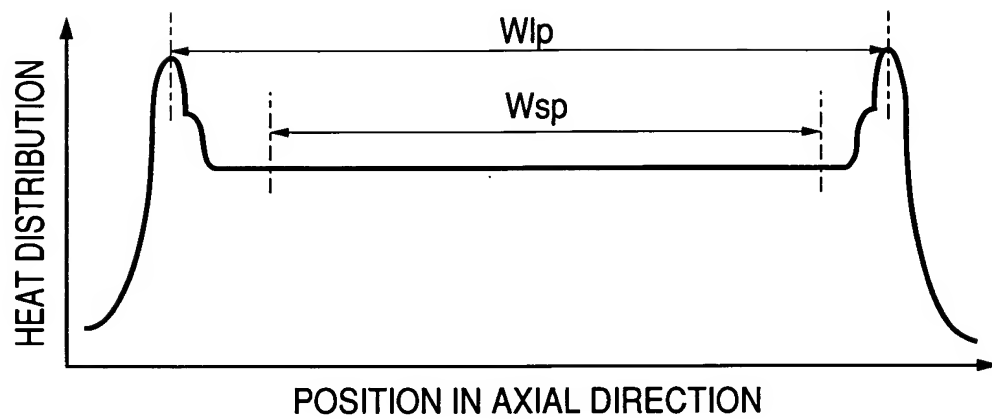


FIG. 7B



**FIG. 8**



**FIG. 9**

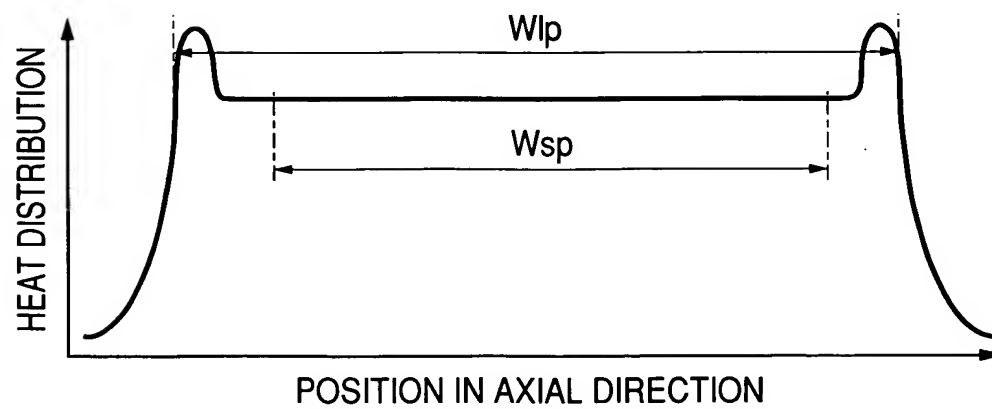
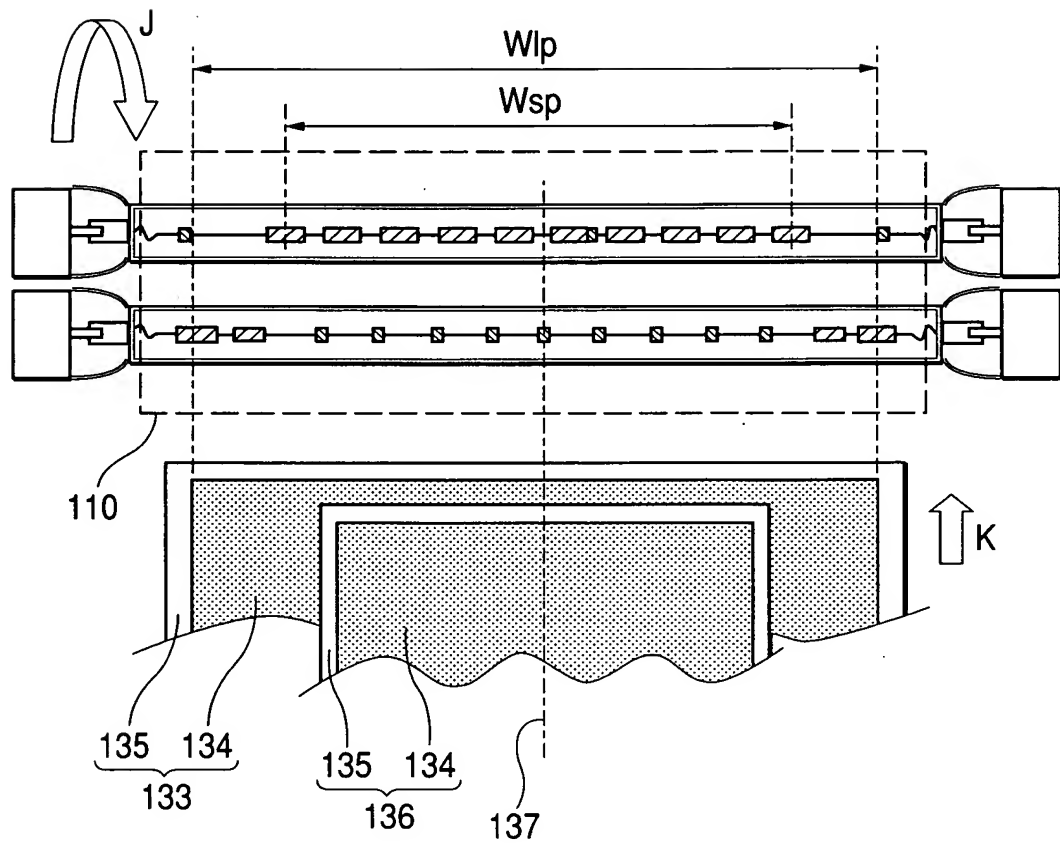
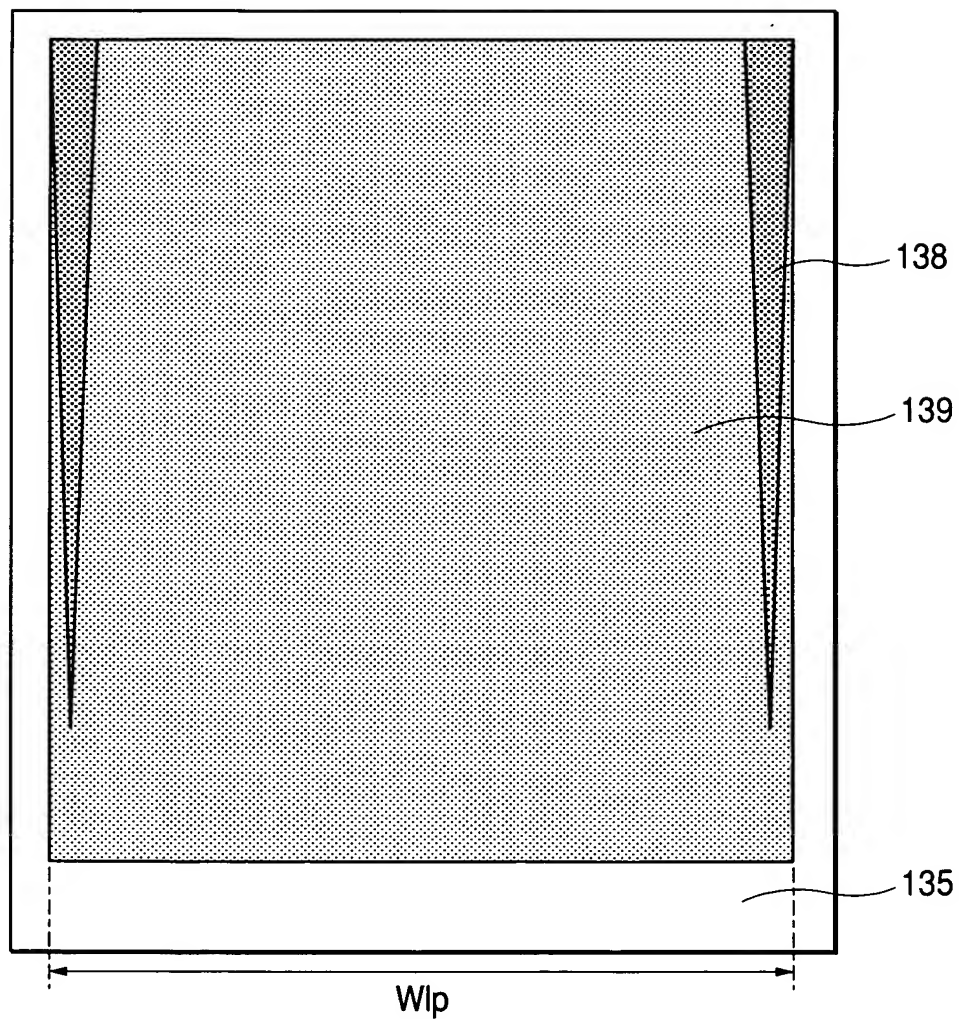


FIG. 10

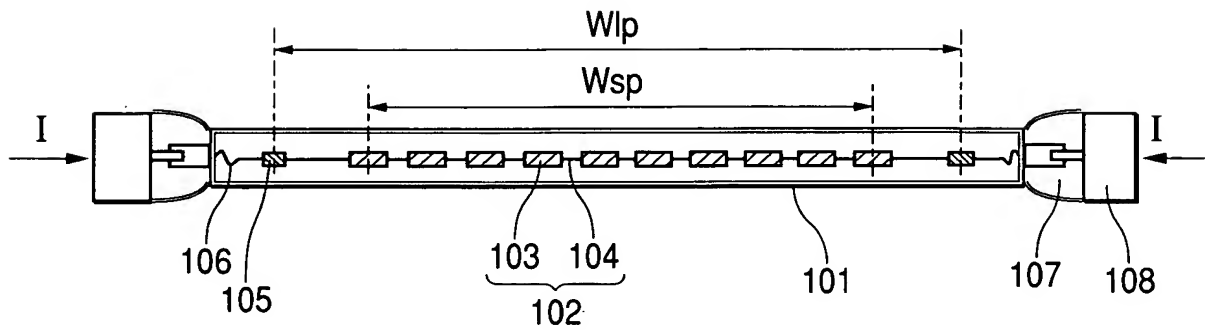


*FIG. 11*

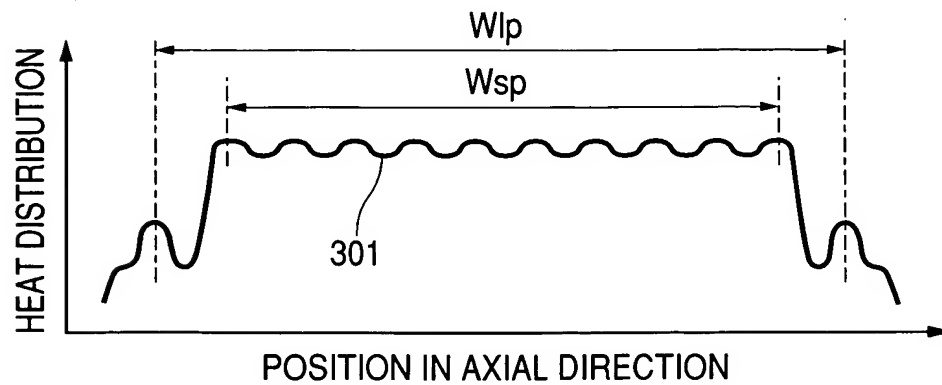




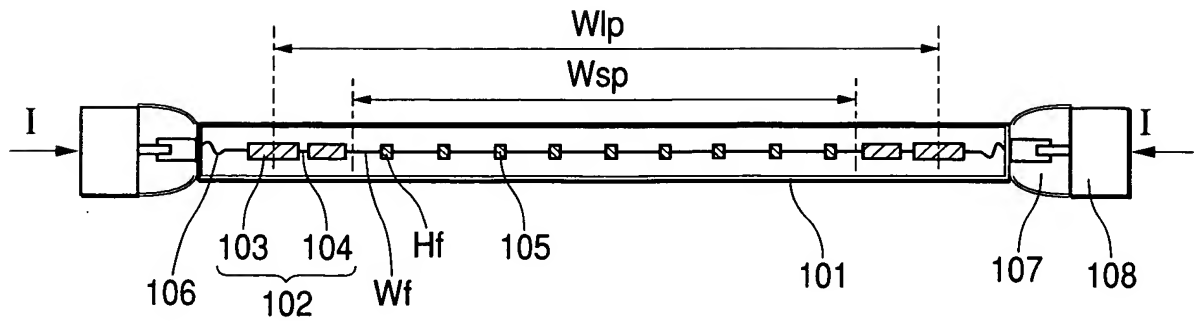
**FIG. 12A**



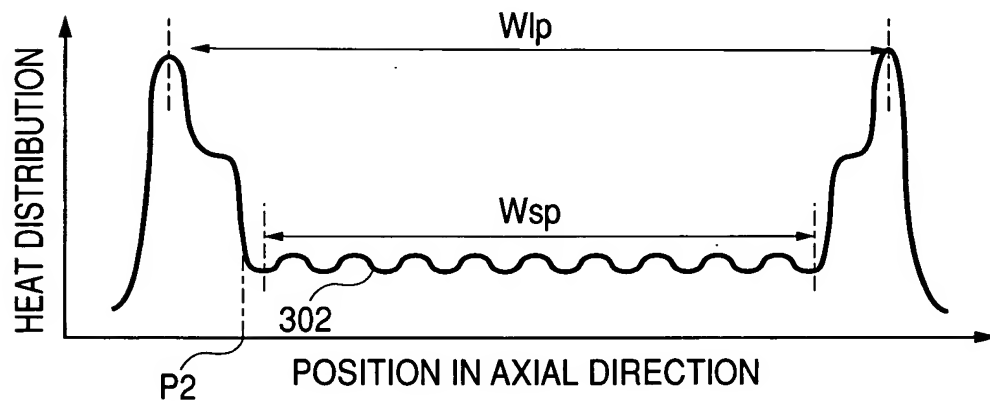
**FIG. 12B**



**FIG. 13A**



**FIG. 13B**



**FIG. 14**

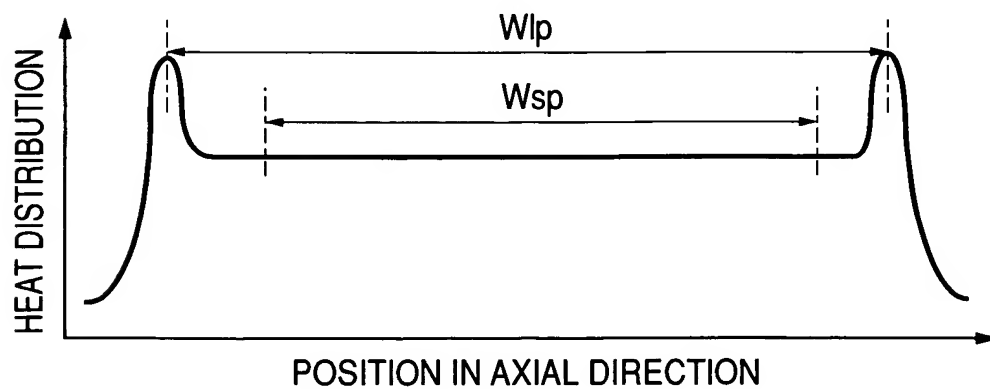


FIG. 15

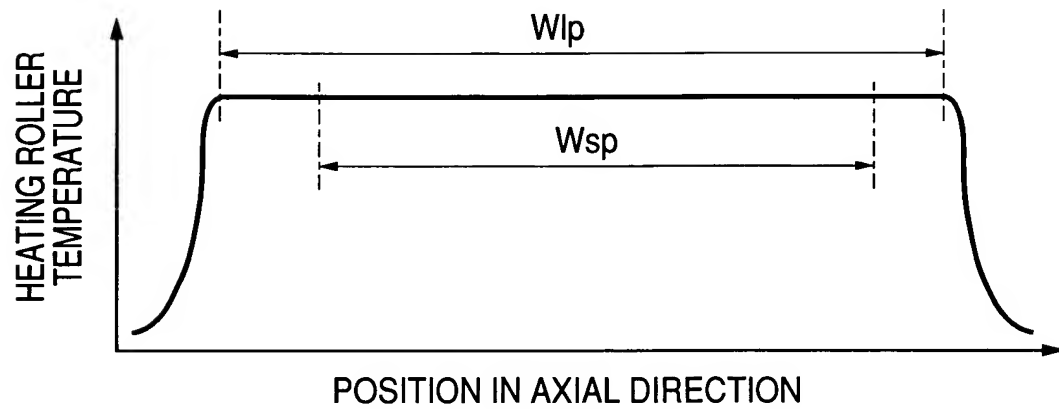


FIG. 16

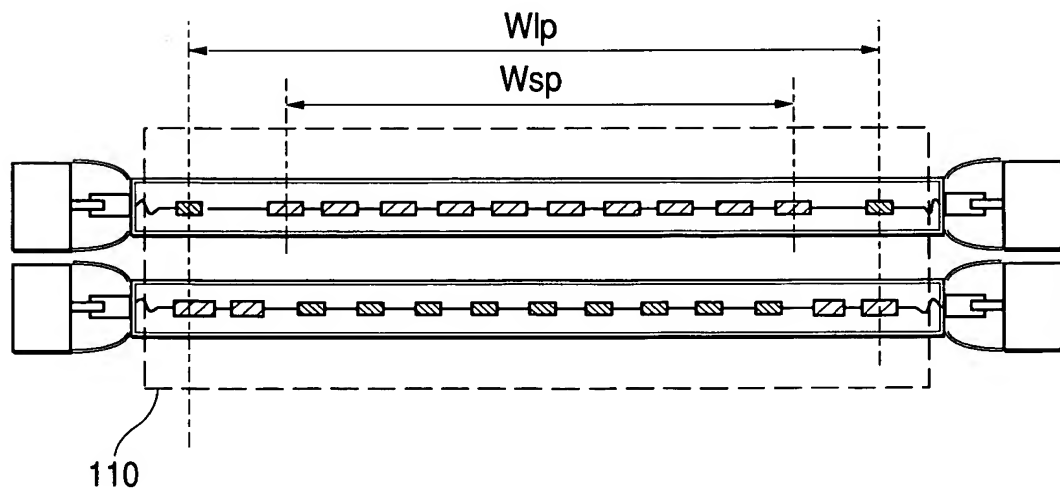


FIG. 17

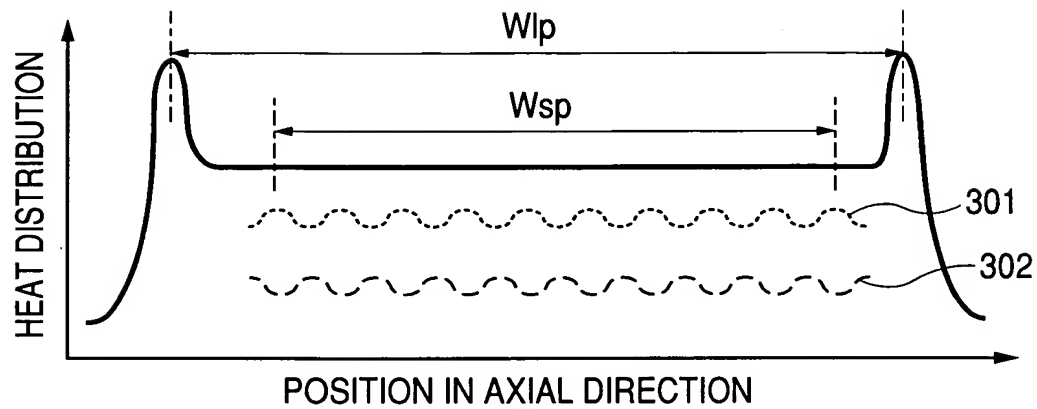


FIG. 18

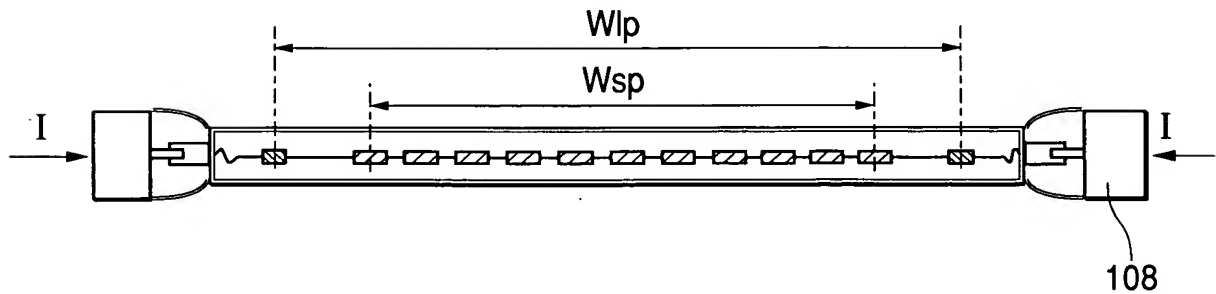


FIG. 19A

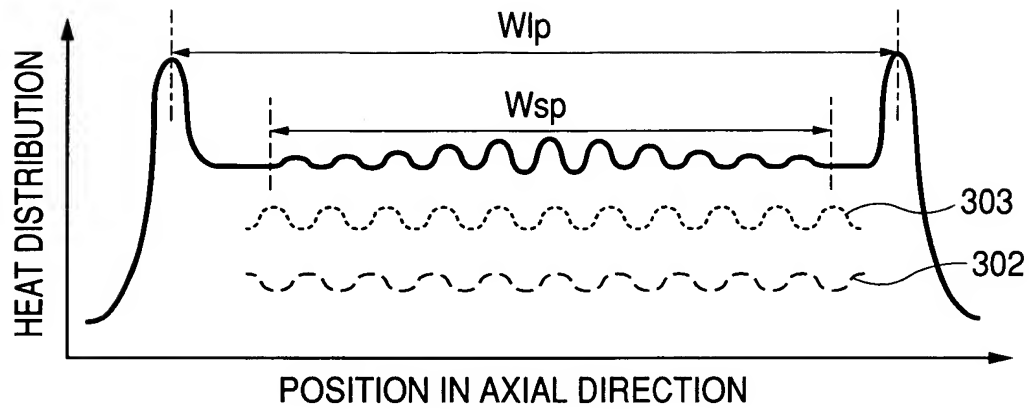


FIG. 19B

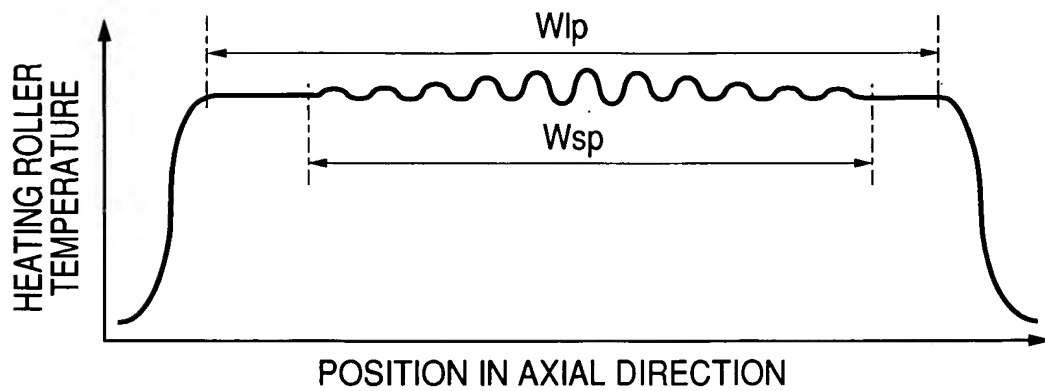


FIG. 20

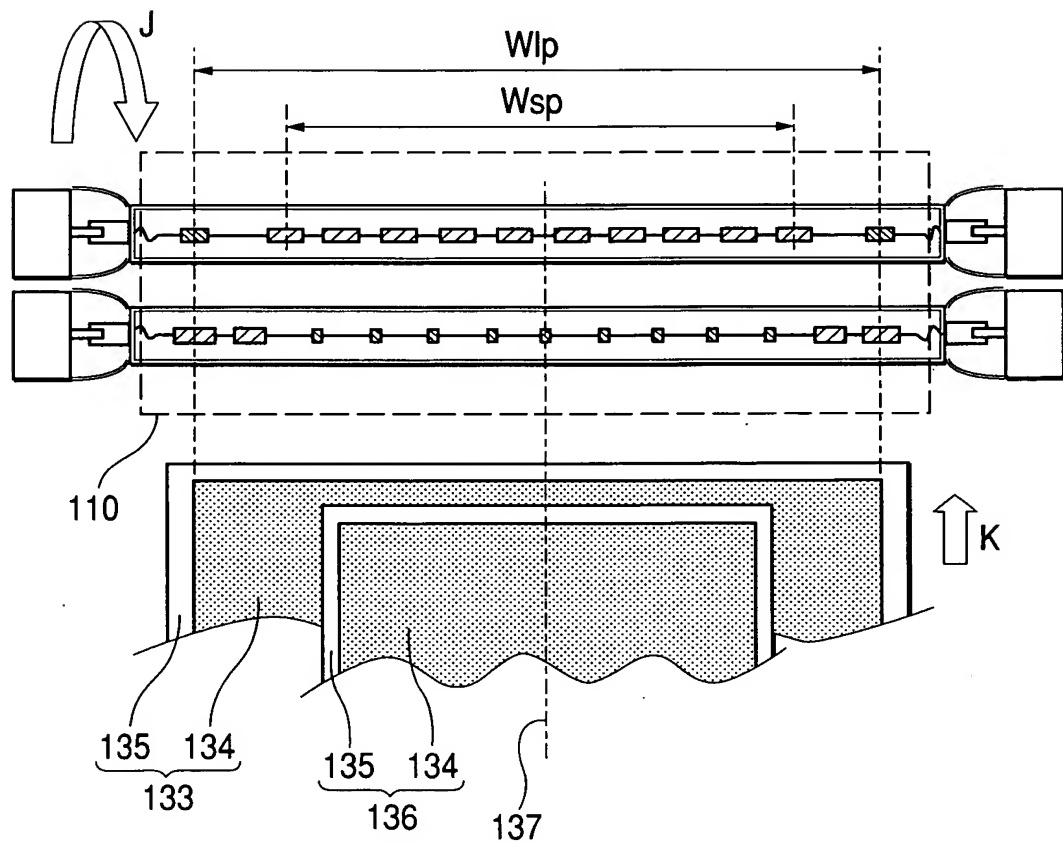


FIG. 21

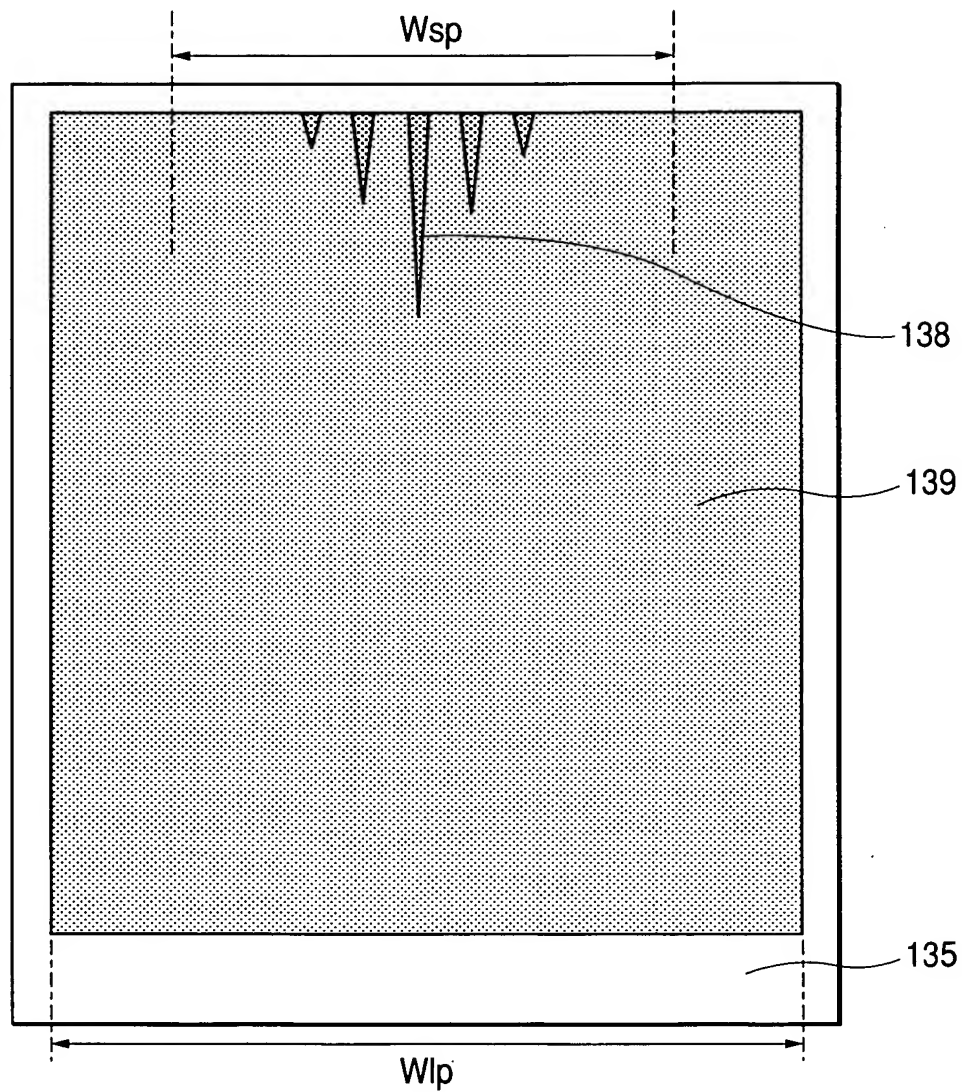


FIG. 22

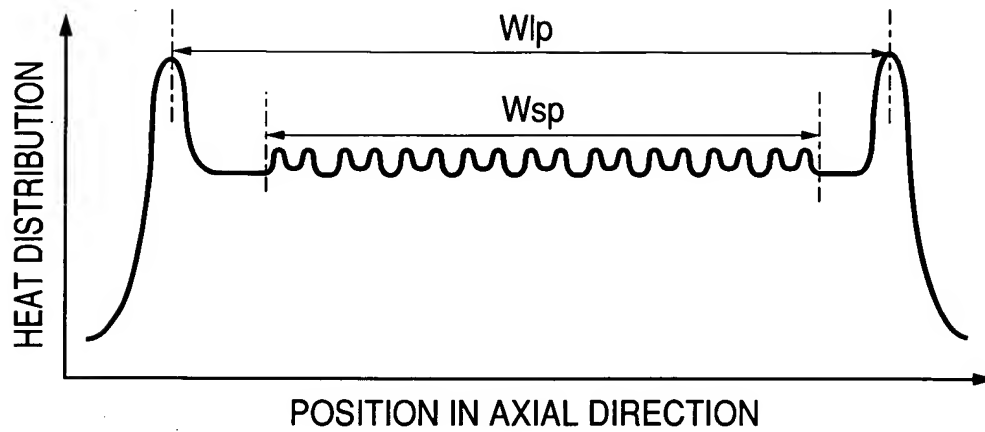


FIG. 23

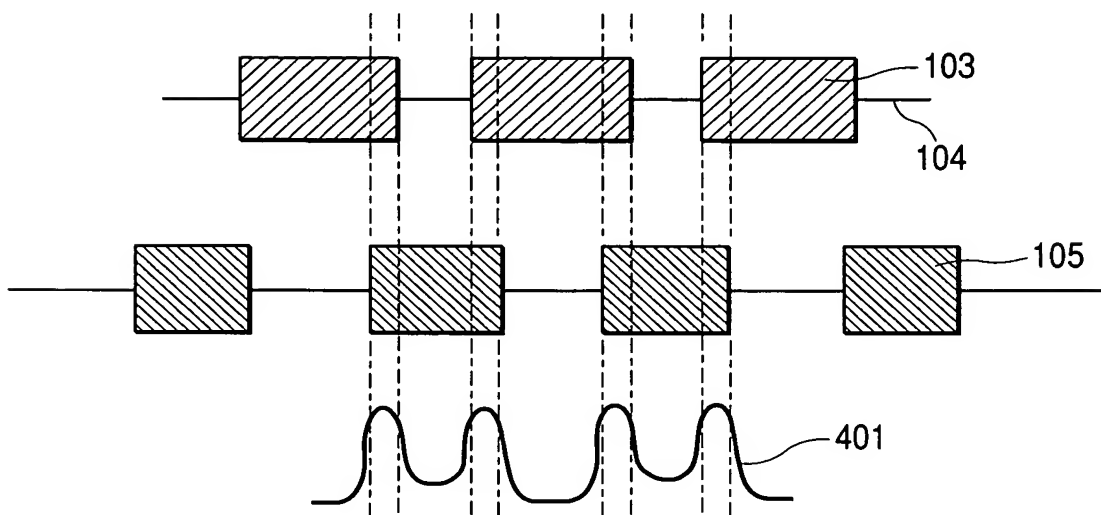




FIG. 24

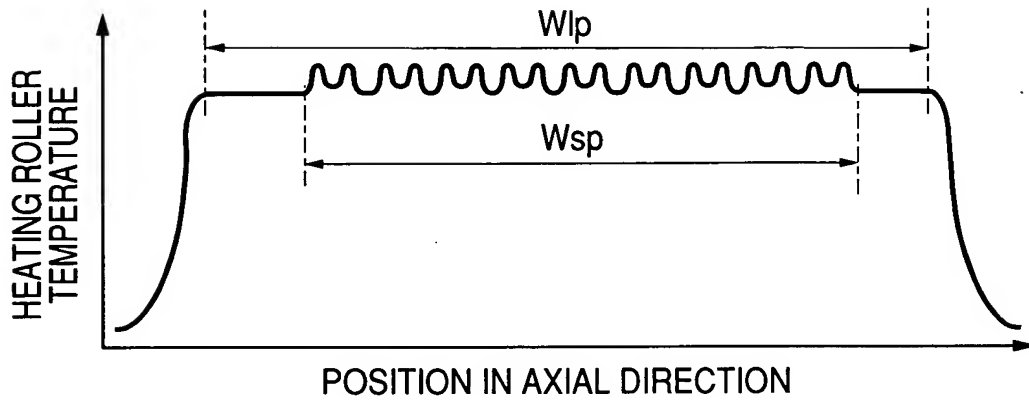
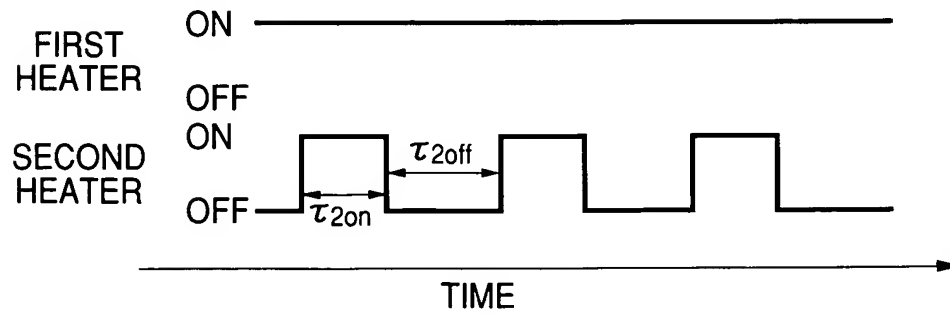


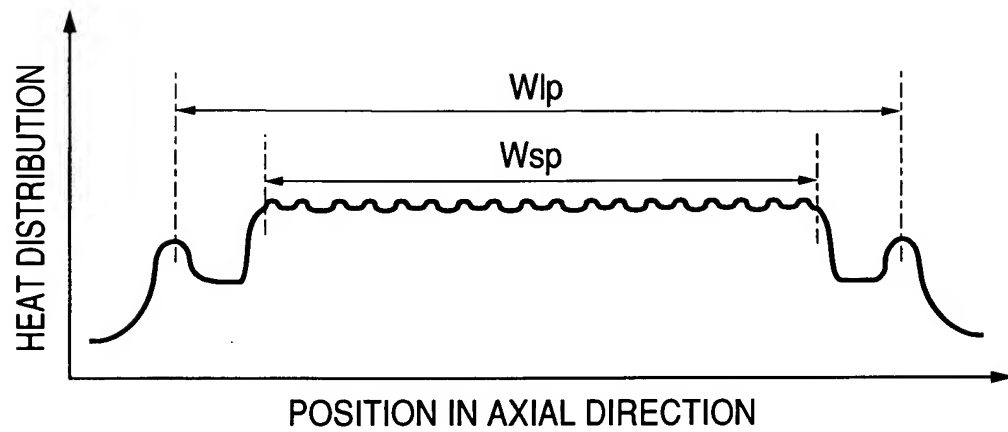
FIG. 25



$$1 = \tau_{1on} / (\tau_{1on} + \tau_{1off})$$

$$0.3 = \tau_{2on} / (\tau_{2on} + \tau_{2off})$$

**FIG. 26A**



**FIG. 26B**

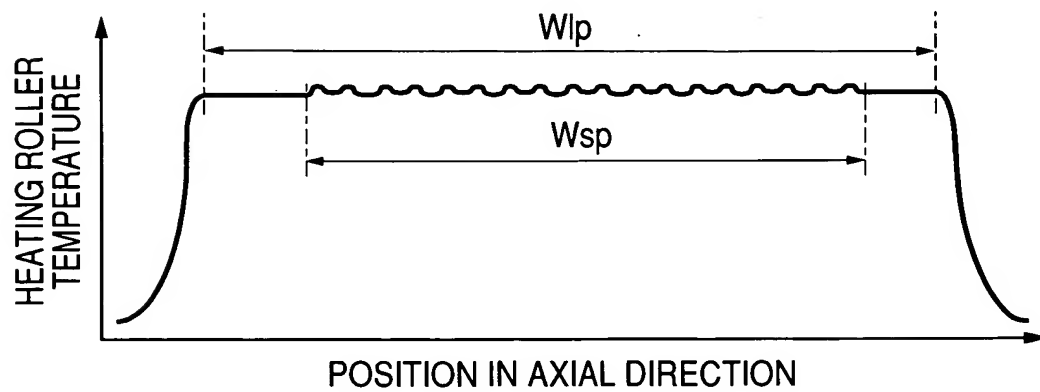


FIG. 27

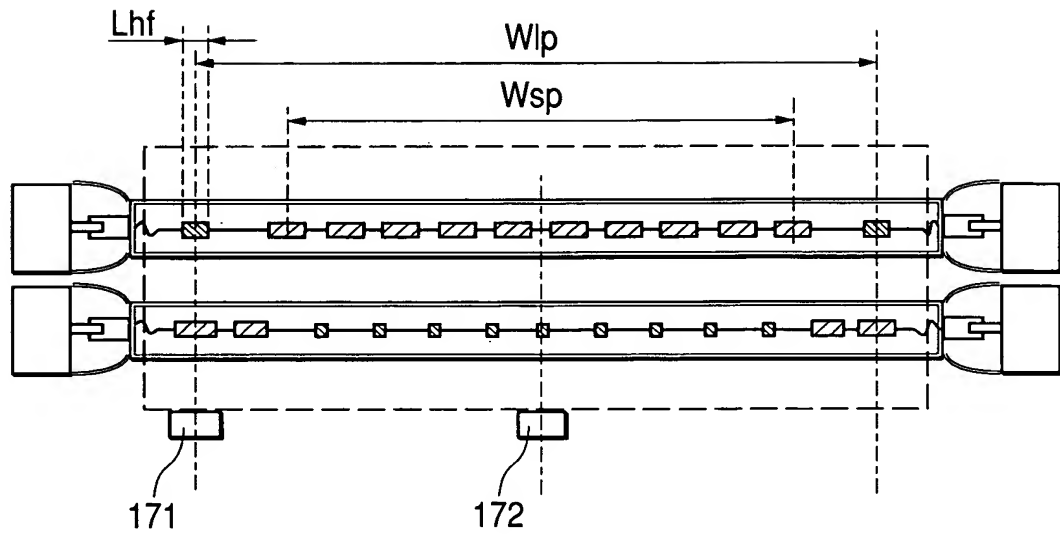


FIG. 28

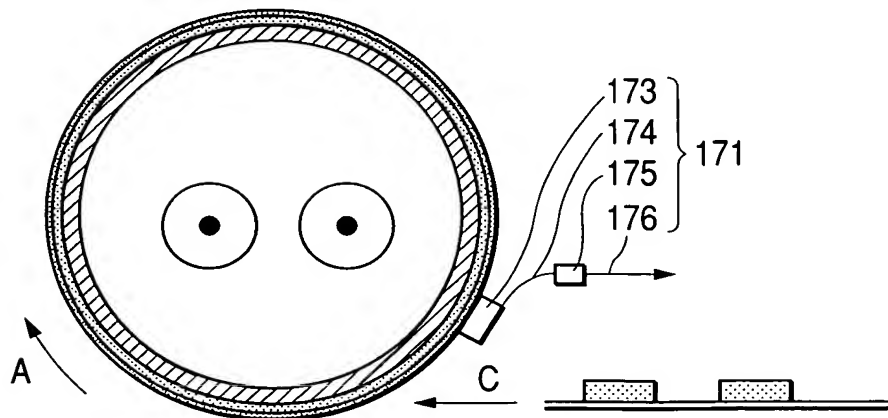


FIG. 29

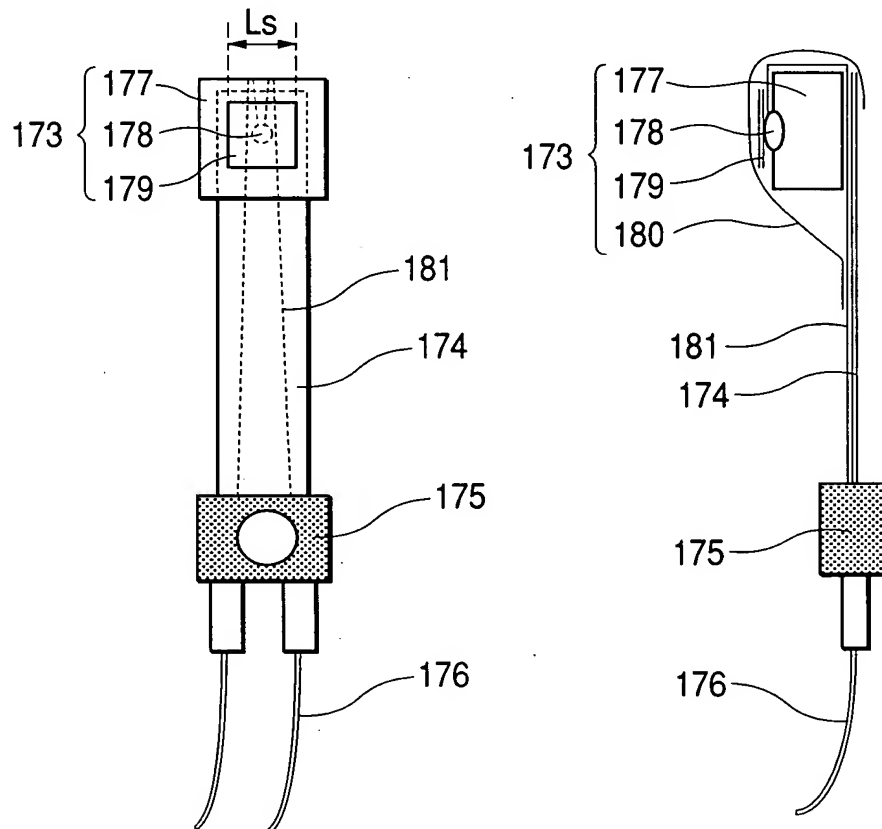
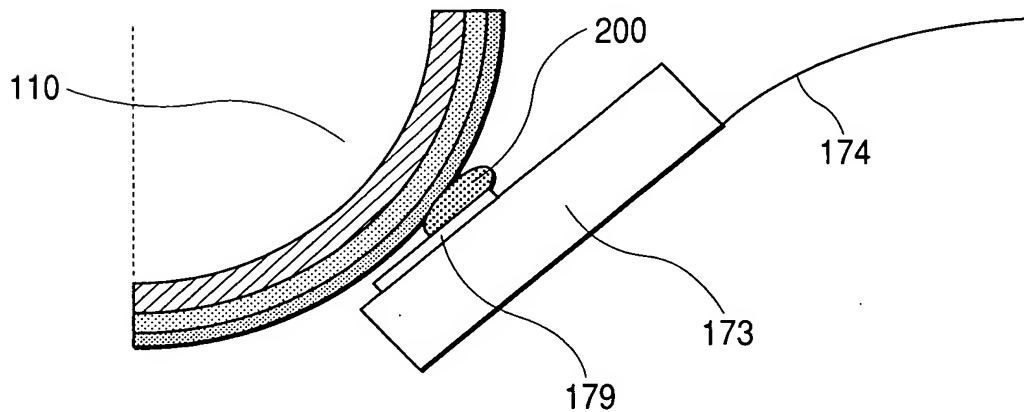
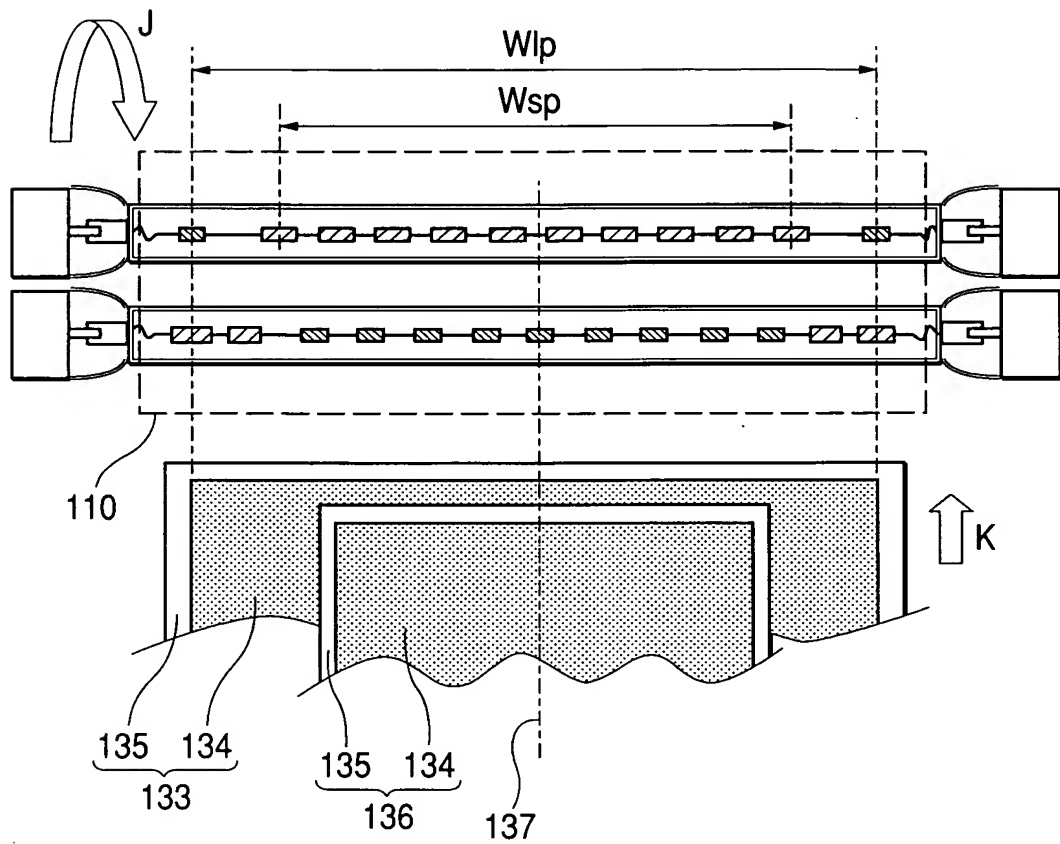


FIG. 30

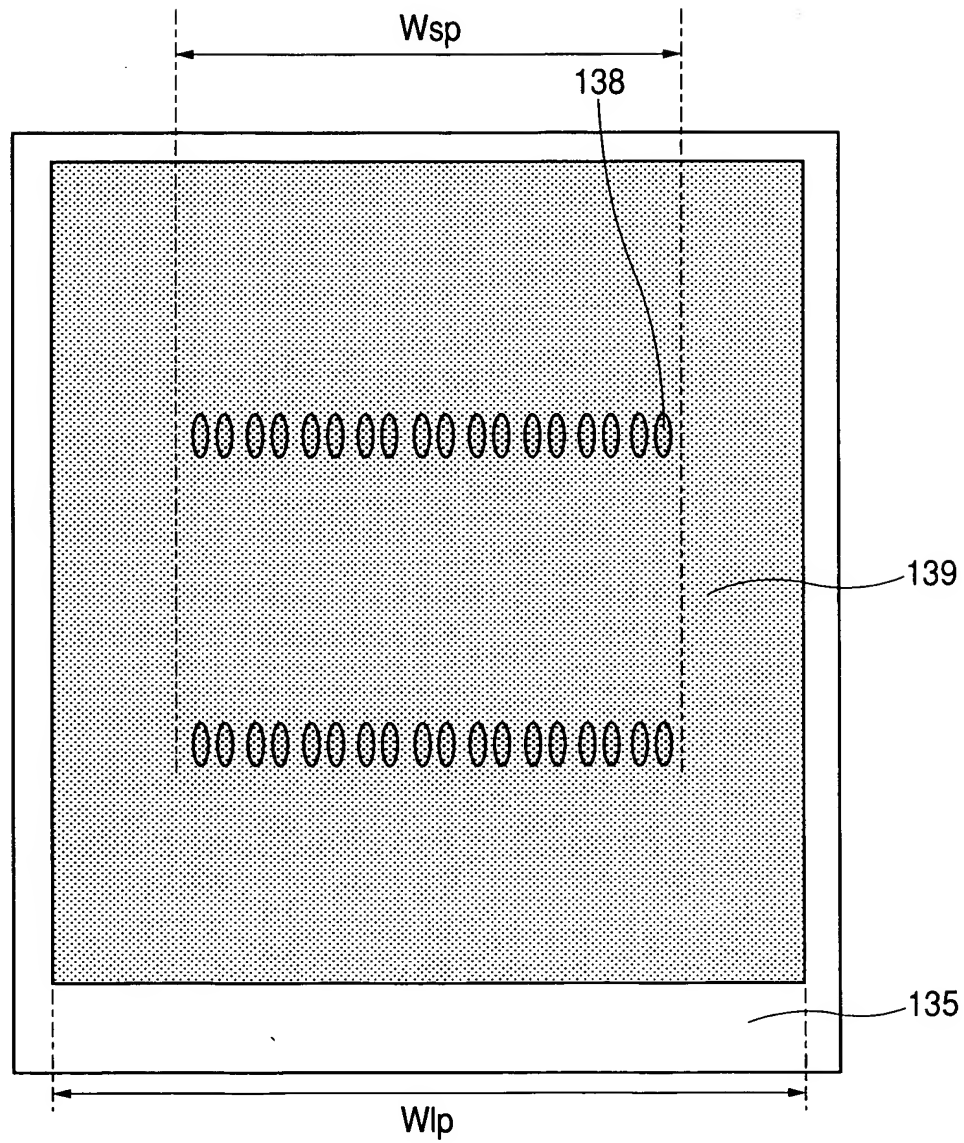


The diagram illustrates the timing of a multi-bit shift register. The top part shows three data bits (D0, D1, D2) being shifted into a 3-bit register. The bottom part shows a clock signal (402) with period  $\Delta T_{ao}$  and a setup time  $\Delta T_{over}$ . The data bits are sampled at the clock edges. The diagram is labeled with 401, 402, 403, and 404.

FIG. 33



*FIG. 34*



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FIG. 35

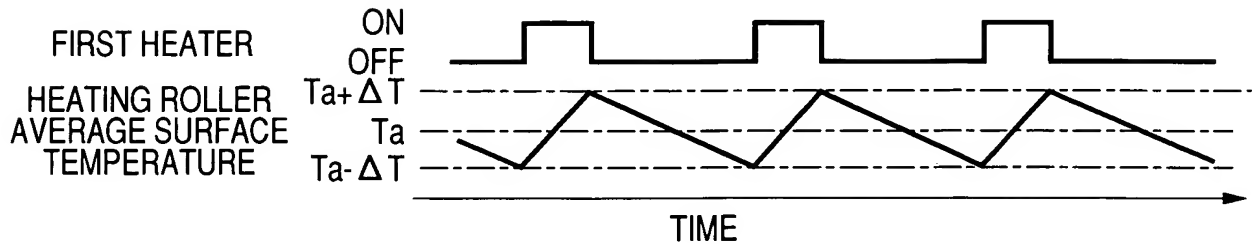


FIG. 36

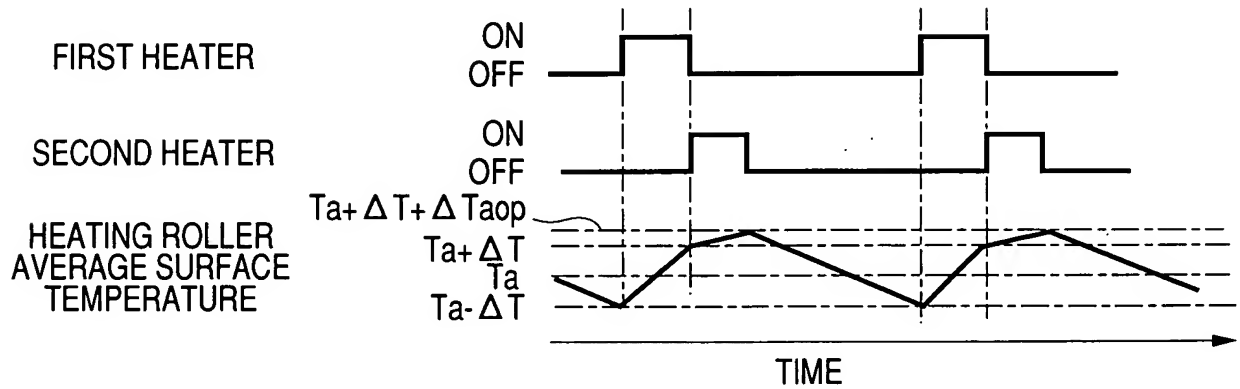


FIG. 37

